TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/917,633
Filing Date	July 31, 2001
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	Thien F. Tran
Examiner Name	2811
Total Number of Pages in This Submission	
Attorney Docket Number	740756-2345

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Declaration and Power of Attorney
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
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- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to Group (Appeal Notice, **Brief (3 original copies)**, Reply Brief)
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Application Data Sheet
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Firm *or* Individual name	**Jeffrey L. Costellia, Reg. No. 35,483** Nixon Peabody LLP 401 9th Street, N.W. Suite 900 Washington, D.C. 20004-2128
Signature	
Date	May 5, 2005

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☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	300	2001	150	Utility filing fee	
1002	200	2002	100	Design filing fee	
1003	200	2003	100	Plant filing fee	
1004	300	2004	150	Reissue filing fee	
1005	200	2005	100	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims	-20** =		X		=	0
Independent Claims	-3** =		X		=	0
Multiple Dependent			X		=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple dependent claim, if not paid
1204	200	2204	100	** Reissue independent claims over original patent
1205	50	2205	25	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	500	2452	250	Petition to revive – unavoidable	
1453	1,500	2453	750	Petition to revive – unintentional	
1501	1,400	2501	700	Utility issue fee (or reissue)	
1502	800	2502	400	Design issue fee	
1503	1,100	2503	550	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

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Date Signature

Typed or printed name

SUBMITTED BY				Complete *(if applicable)*	
Name *(Print/Type)*	Jeffrey L. Costellia	Registration No. *(Attorney/Agent)*	35,483	Telephone	(202) 585-8000
Signature				Date	May 5, 2005

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Attorney Docket No. 740756-2345

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re PATENT application of	)	
Shunpei YAMAZAKI et al.	)	Confirmation No.: 3382
Application No. 09/917,633	)	Group Art Unit: 2811
Filed: July 31, 2001	)	Examiner: Thien F. Tran
For: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	)	May 5, 2005

APPEAL BRIEF

Mail Stop **Appeal Brief – Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed April 7, 2005.

05/06/2005 JADD01 00000023 09917633
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I. REAL PARTY IN INTEREST

Semiconductor Energy Laboratory Co., Ltd. is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are presently no appeals or interferences known to the Appellants, the Appellants' representative, or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-13 are currently pending in the application. This Appeal is taken from the rejection of claims 1-13, as submitted in the Appendix herewith.

IV. STATUS OF AMENDMENTS

No amendments have been made to the claims since filing. The pending claims are allowable over the applied references, as argued herein.

V. SUMMARY OF INVENTION

A semiconductor device and associated method of fabricating are disclosed in accordance with exemplary embodiments of the invention set forth in the present specification. Conventionally, a crystalline semiconductor thin film used for thin film devices such as a thin film insulated gate type field effect transistor (TFT) has been fabricated by crystallizing an amorphous silicon film formed by a plasma CVD method or thermal CVD method at a temperature of more than 600° C in an apparatus such as an electric furnace (see specification, page 1, lines 8-13).

This conventional method, however, has had problems. For example, it is difficult to obtain a quality product since the crystalline silicon film obtained during transistor fabrication is polycrystal which results in difficultly in controlling its grain boundary. Also, the film's reliability and yield is not sufficiently high because of its dispersion characteristic. In other words, because the silicon crystals obtained by conventional heat treatment grow at random, it is almost impossible to control the direction of its crystal growth (see specification, page 1, lines 14-22).

Thus, in accordance with the exemplary embodiments of the present invention, crystal growth is controlled to thereby provide a transistor having high quality crystalline silicon film. FIGs. 1-4 illustrate the process by which the transistor is formed.

In accordance with one exemplary embodiment of the present invention a transistor is provided that includes a plurality of metal advanced crystallization regions. Specifically, the transistor includes a metal advanced lateral crystallization region formed on a substrate with a semiconductor material and including a channel region (see specification, page 6, lines 3-10; see also Evidence Appendix). The transistor also includes a plurality of metal advanced crystallization regions formed on sides of the metal advanced lateral crystallization region with a semiconductor material (see specification page 7, lines 16-22 and FIG. 1B; see also Evidence Appendix). At least one boundary between the metal advanced lateral crystallization region and one of the metal advanced crystallization regions is located outside the channel region (see specification, page 9, lines 15-19 and FIGs. 1A-1C; see also Evidence Appendix). As a result of the controlled crystal growth, a transistor having a high quality crystalline silicon film is provided.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on appeal are as follows:

Claims 1-13 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellants regard as the invention.

VII. ARGUMENT

A. The Rejection of Claims 1-13 Under 35 U.S.C. § 112, First Paragraph, as Failing to Comply With the Written Description Requirement, Should Be REVERSED

Claims 1-13 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Appellants appeal this rejection and request reversal for at least the following reasons.

Appellants contend that the presently pending claims include sufficient support by the specification to satisfy the requirements of Section 112, first paragraph, written description requirement. Support for all of the claim language is provided in the *Request for Interference Under 37 C.F.R. 1.607* filed on May 29, 2002. A copy of this claim chart, referenced during prosecution of the present application is attached hereto in the Evidence Appendix. Appellants submit that, as can be seen from this chart, there is clearly adequate support for each any every claim limitation. In particular support in the specification is provided for the features "a metal advanced lateral crystallization region" in claims 1-5 and 9-11; "a plurality of metal advanced crystallization regions" in claims 1 and 10; "a metal advanced crystallization region" in claims 6-7 and 9; "a metal induced lateral crystallization region" in claims 12-13 and "a plurality of metal induced crystallization regions" in claim 12, that are noted by the Examiner in the rejection. Moreover, the specification is very detailed on how the regions are formed and what occurs in each region during formation.

Appellants submit that the Examiner has failed to meet the initial burden required by the case law. Specifically, the Examiner does not set forth a specific, detailed reasoning for the rejection, i.e., point out where support is clearly filed. See, M.P.E.P. 2163.02 and 2163.04 which state:

> The courts have described the essential question to be addressed in a description requirement issue in a variety of ways. An objective standard for determining compliance with the written description requirement is, "does the description clearly allow persons of ordinary skill in the art to recognize that he or she invented what is claimed." *In re Gosteli*, 872 F.2d 1008, 1012, 10 USPQ2d 1614, 1618 (Fed. Cir. 1989). Under *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991), to satisfy the

> written description requirement, an Appellant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention, and that the invention, in that context, is whatever is now claimed. The test for sufficiency of support in a parent application is whether the disclosure of the application relied upon "reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter." *Ralston Purina Co. v. Far-Mar-Co., Inc.*, 772 F.2d 1570, 1575, 227 USPQ 177, 179 (Fed. Cir. 1985) (quoting In re Kaslow, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983)).
>
> The inquiry into whether the description requirement is met must be determined on a case-by-case basis and is a question of fact. *In re Wertheim*, 541 F.2d 257, 262, 191 USPQ 90, 96 (CCPA 1976). A description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. See, e.g., *In re Marzocchi*, 439 F.2d 220, 224, 169 USPQ 367, 370 (CCPA 1971). The examiner, therefore, must have a reasonable basis to challenge the adequacy of the written description. The examiner has the initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize in an Appellant's disclosure a description of the invention defined by the claims. *Wertheim*, 541 F.2d at 263, 191 USPQ at 97.

Moreover, the case law set forth in M.P.E.P. 2111.01 clearly allows the Appellant to be his own lexicographer in drafting the claims.

> Applicant may be his or her own lexicographer **>; however any special< meaning assigned to *>a< term ** "must be sufficiently clear in the specification that any departure from common usage would be so understood by a person of experience in the field of the invention." *Multiform Desiccants Inc. v. Medzam Ltd.*, 133 F.3d 1473, 1477, 45 USPQ2d 1429, 1432 (Fed. Cir. 1998). >See also *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999) and MPEP § 2173.05(a) <2100_2173_05_a.htm>.< as long as terminology is supported by the specification.

Further, the Federal Circuit in *Union Oil Co. of California v. Atlantic Richfield Co.*, 208 F3d 989, 54 USPQ2s 1227; (Fed. Cir. 2000) relies heavily on Wertheim and makes it clear that precise recitation of the claim limitation in the disclosure is not requirement for "written description" to be satisfied, i.e., the invention does not have to be described *ipsis verbis* in order to satisfy the description requirement of section

112. In view of the foregoing, it is believed that the rejection under Section 112, first paragraph, should be withdrawn.

Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Clearly, the specification provides support for this feature on page 7, lines 15-16, and in Figures 1B, 3B, 3C and 4C. The disclosure surrounding this features also provides the manner in which one of skill in the art can accomplish this feature, particularly when viewing Figures 3B and 3C. As a result, this rejection should likewise be overcome.

Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Support for these features are clearly provided in the attached claim chart (located in the Evidence Appendix). For the reasons advanced above with respect to claims 1-13, one of skill in the art would clearly have sufficient disclosure in the specification to permit formation of the recited transistor.

Appellants also note the Examiner has failed to expressly address Appellants' arguments provided in Responses by Appellants during prosecution of this application such that it is entirely unclear why the rejection is being maintained. As an example, Appellants note that the Office Action of March 1, 2004 provided the initial rejection under 35 U.S.C. 112, first paragraph. The Examiner in the Office Action provided an explanation for the rejection as follows:

> The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claims require essential or critical features which are not adequately described in the specification and which are not conventional in the art or known to one of ordinary skill in the art. For example, consider the features ua metal advanced lateral crystallization region" in claims 1-5 and 9-11; "a plurality of metal advanced crystallization regions" in claims 1 and I 0; "a metal advanced crystallization region" in claims 6-7 and 9; "a metal induced lateral crystallization region" in claims 12-13; and "a plurality of metal induced crystallization regions" in claim 12. There is insufficient description of these specific features in the specification that the knowledge and level of skill in the art would not permit one skilled in the art immediately envisage the product claimed from the disclosed process.

In the response to the Office Action filed August 2, 2004, Appellants provided argument as well as another copy of the detailed claim chart (supplied herewith as Evidence Appendix) which provides specific support within the specification for each feature of each claim in the application. More importantly, the claim chart provides specific support for each alleged inadequately described feature cited by the Examiner.

In response to the Request for Reconsideration filed by Appellants, an Office Action, dated October 13, 2004, containing the exact rejection as in the Office Action dated March 1, 2004 was issued. The wording of the rejection was exactly the same as in the Office Action of March 1, 2004. Appellants note that the Examiner did not make any effort to rebut **any** of the citations provided in the claim chart provided by Appellants. Nor did the Examiner elaborate or provide **any** reasoning as to why the rejection was being maintained. In view of the detailed support in the pending application provided in the claim chart provided to the Examiner and the utter lack of response by the Examiner, Appellants respectfully request reconsideration and withdrawal of the rejection. Accordingly, it is respectfully requested that this rejection be reconsidered and withdrawn.

B. The Rejection of Claims 1-13, Under 35 U.S.C. § 112, Second Paragraph, as Being Indefinite for Failing to Particularly Point Out and Distinctly Claim the Subject Matter Which Appellants Regard as the Invention, Should Be REVERSED

Claims 1-13 are also rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellant regards as the invention.

The Examiner argues that since the specification does not provide an adequate description of "a metal advanced lateral crystallization region" in claims 1-5 and 9-11; "a plurality of metal advanced crystallization regions" in claims 1 and 10; "a metal advanced crystallization region" in claims 6-7 and 9; "a metal induced lateral crystallization region" in claims 12-13 and "a plurality of metal induced crystallization regions" in claim 12, the claims are indefinite. Appellants respectfully

submit that this rejection is not proper under second paragraph since these terms, in view of their descriptiveness and support within the specification discussed above, are definite on their face. Moreover, like the rejection discussed above, Appellants note that the Examiner did not make any effort to rebut **any** of the arguments or citations provided by Appellants, nor did the Examiner elaborate or provide **any** reasoning as to why the rejection was being maintained. Therefore, this rejection should likewise be overcome.

Conclusion

The rejection of claims 1-13 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement, should be reversed. The Examiner has provided an insufficient factual basis to support a the rejection.

Accordingly, the rejection of claims 1-13 are in error and reversal thereof is respectfully requested.

Respectfully submitted,

NIXON PEABODY, LLP

Date: May 5, 2005

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VIII. CLAIMS APPENDIX

The following is a complete list of all claims in this application.

1. (Original) A transistor comprising:

a metal advanced lateral crystallization region formed on a substrate with a semiconductor material and including a channel region; and

a plurality of metal advanced crystallization regions formed on sides of the metal advanced lateral crystallization region with a semiconductor material, wherein at least one boundary between the metal advanced lateral crystallization region and one of the metal advanced crystallization regions is located outside the channel region.

2. (Original) The transistor according to claim 1, wherein the metal advanced lateral crystallization region include impurity doped regions formed on sides of the channel region.

3. (Original) The transistor of claim 1, wherein the metal advanced lateral crystallization region includes source and drain regions.

4. (Original) The transistor of claim 1, wherein the metal advanced lateral crystallization region includes no dopant portions formed on sides of the channel region.

5. (Original) A transistor comprising:

a channel region;

a source region having a first source portion adjacent to the channel region and a second source portion adjacent to the first source portion; and

a drain region having a first drain portion adjacent to the channel region and a second drain portion adjacent to the first drain portion;

wherein the channel region and at least one of the first source portion and the first drain portion comprise a metal advanced lateral crystallization region.

6. (Original) The transistor of claim 5, wherein the second source portion comprises a metal advanced crystallization region.

7. (Original) The transistor of claim 5, wherein the second drain portion comprises a metal advanced crystallization region.

8. (Original) The transistor of claim 5, wherein the source and drain regions are impurity doped.

9. (Original) The transistor of claim 5, wherein the channel region, the first source portion and the first drain portion comprise the metal advanced lateral crystallization region, the second source region comprises a metal advanced crystallization region, and the second drain region comprises a metal advanced crystallization region.

10. (Original) A transistor comprising:

a metal advanced lateral crystallization region formed on a substrate with a semiconductor material and including a channel region; and

a plurality of metal advanced crystallization regions formed on sides of the metal advanced lateral crystallization region with a semiconductor material, wherein at least one portion between the metal advanced lateral crystallization region and one of the metal advanced crystallization regions is located outside the channel region.

11. (Original) A transistor comprising:

a channel region;

a source region having a source portion adjacent to the channel region; and

a drain region having a drain portion adjacent to the channel region;

wherein the channel region and at least one of the source portion and the drain portion comprise a metal advanced lateral crystallization region.

12. (Original) A transistor comprising:

a metal induced lateral crystallization region formed on a substrate with a semiconductor material and including a channel region; and

a plurality of metal induced crystallization regions formed on sides of the metal induced lateral crystallization region with a semiconductor material, wherein at least one boundary between the metal induced lateral crystallization region and one of the metal induced crystallization regions is located outside the channel region.

13. (Original) A transistor comprising:

a channel region;

a source region having a first source portion adjacent to the channel region and a second source portion adjacent to the first source portion; and

a drain region having a first drain portion adjacent to the channel region and a second drain portion adjacent to the first drain portion;

wherein the channel region and at least one of the first source portion and the first drain portion comprise a metal induced lateral crystallization region.

IX. EVIDENCE APPENDIX

Claim Language	Support in Pending Application
1. A transistor comprising:	The present invention relates to a method of obtaining... (thin film transistor or TFT) (page 1, lines 5-8); The TFT . . .was fabricated through the process described above. (page 7, line 32 – page 8, line 1)
a metal advanced lateral crystallization region	"forming regions containing at least one of nickel,... so that they adhere on part of the impurity regions, and by annealing the whole to crystallize it starting from the region containing nickel" (page 2, lines 8-11). "advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17). "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction with the surface of the substrate" (page 24, lines 2-3).
formed on a substrate	substrate . . . 10 (page 6, line 11).
with a semiconductor material	title; "an amorphous silicon film" (page 6, line 12)
and including a channel region; and	"channel forming region (the semiconductor region under the gate) electrode" (page 8, lines 8-9) (Fig. 1)
a plurality of metal advanced crystallization regions formed on sides of the metal advanced lateral crystallization region with a semiconductor material,	"[H]oles were created on the silicon oxide file 13 on the impurity regions to form nickel silicide (or nickel) films 17A and 17B . . . Then annealing was carried out . . to crystallize the impurity regions 16 and other semiconductor

	regions." (Fig. 1; page 7 lines 16-22).
wherein at least one boundary between the metal advanced lateral crystallization region and one of the metal advanced crystallization regions is located outside the channel region.	"[T]he present invention allows substantial elimination of the grain boundary between the source and drain and the active layer... by advancing the crystallization of the source and drain at the same time as crystallization of the active layer (channel forming region)." (page 2, lines 12-17); "According to the present invention,... the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18); "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)).
2. The transistor according to claim 1, wherein the metal advanced lateral crystallization region	Claim 1.
include (sic) impurity doped regions	[A]n impurity was introduced by a plasma doping method. . . . Impurity regions 16A and 16B were thus formed. (page 7, lines 10-15, Figure 1B).
formed on sides of the channel region.	"[H]oles were created on the silicon oxide file 13 on the impurity regions to form nickel silicide (or nickel) films 17A and 17B . . . Then annealing was carried out . . to crystallize the impurity regions 16 and other semiconductor regions." (Fig. 1; page 7 lines 16-22).
3. The transistor of claim 1, wherein the metal advanced lateral crystallization region	Claim 1.
includes source and drain regions.	"advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17.)
4. The transistor of claim 1, wherein the metal advanced lateral crystallization region includes no dopant portions formed on sides of the channel region.	"The impurity regions and the gate electrode were offset as seen in the figure." (page 7, lines 15-16; Figures 1B; 3B; 3C; 4)
5. A transistor comprising:	The present invention relates to a method of obtaining... (thin film transistor or TFT) (page 1, lines 5-8); The TFT . . .was fabricated through the process described above. (page 7, line 32 – page 8, line 1)
a channel region;	"channel forming region (the semiconductor region under the gate) electrode" (page 8, lines

	8-9) (Fig. 1)
a source region	"the source" (page 8, line 7).
having a first source portion adjacent to the channel region and a second source portion adjacent to the first source portion;	"[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)). Thus, any "grain boundary" exists in the source portion and defines the first source portion and the second source portion.
and a drain region having a first drain portion adjacent to the channel region and a second drain portion adjacent to the first drain portion;	"[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)). Thus, any "grain boundary" exists in the drain portion and defines the first drain portion and the second drain portion.
wherein the channel region and at least one of the first source portion and the first drain portion comprise a metal advanced lateral crystallization region.	"[T]heir direction of crystallization is the same. (page 8, lines 9-10) "advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17.) "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to

	the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction with the surface of the substrate" (page 24, lines 2-3).
6. The transistor of claim 5, wherein the second source portion comprises a metal advanced crystallization region.	"[A]dvancing the crystallization of the source and drain" (page 2, line 15). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "[C]rystals are grown in the vertical direction with the surface of the substrate from the lower side of the semiconductor to the upper side thereof or vice versa." (page 24, lines 3-5).
7. The transistor of claim 5, wherein the second drain portion comprises a metal advanced crystallization region.	"[A]dvancing the crystallization of the source and drain" (page 2, line 15). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "[C]rystals are grown in the vertical direction with the surface of the substrate from the lower side of the semiconductor to the upper side thereof or vice versa." (page 24, lines 3-5).
8. The transistor of claim 5, wherein the source and drain regions are impurity doped.	[A]n impurity was introduced by a plasma doping method. . . . Impurity regions 16A and 16B were thus formed. (page 7, lines 10-15, Figure 1B).
9. The transistor of claim 5, wherein the channel region, the first source portion and the first drain portion comprise the metal advanced lateral crystallization region,	"advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17). "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of

	crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction with the surface of the substrate" (page 24, lines 2-3).
the second source region comprises a metal advanced crystallization region,	"[A]dvancing the crystallization of the source and drain" (page 2, line 15). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "[C]rystals are grown in the vertical direction with the surface of the substrate from the lower side of the semiconductor to the upper side thereof or vice versa." (page 24, lines 3-5).
and the second drain region comprises a metal advanced crystallization region.	"[A]dvancing the crystallization of the source and drain" (page 2, line 15). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "[C]rystals are grown in the vertical direction with the surface of the substrate from the lower side of the semiconductor to the upper side thereof or vice versa." (page 24, lines 3-5).
10. A transistor comprising:	The present invention relates to a method of obtaining... (thin film transistor or TFT) (page 1, lines 5-8); The TFT . . .was fabricated through the process described above. (page 7, line 32 – page 8, line 1)
a metal advanced lateral crystallization region	"forming regions containing at least one of nickel,... so that they adhere on part of the impurity regions, and by annealing the whole to crystallize it starting from the region containing nickel" (page 2, lines 8-11). "advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17). "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present

	invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction with the surface of the substrate" (page 24, lines 2-3).
formed on a substrate	substrate . . . 10 (page 6, line 11).
with a semiconductor material	title; "an amorphous silicon film" (page 6, line 12)
and including a channel region; and	"channel forming region (the semiconductor region under the gate) electrode" (page 8, lines 8-9) (Fig. 1)
a plurality of metal advanced crystallization regions formed on sides of the metal advanced lateral crystallization region with a semiconductor material,	"[H]oles were created on the silicon oxide file 13 on the impurity regions to form nickel silicide (or nickel) films 17A and 17B . . . Then annealing was carried out . . to crystallize the impurity regions 16 and other semiconductor regions." (Fig. 1; page 7 lines 16-22).
wherein at least one portion between the metal advanced lateral crystallization region and one of the metal advanced crystallization regions is located outside the channel region.	"[T]he present invention allows substantial elimination of the grain boundary between the source and drain and the active layer... by advancing the crystallization of the source and drain at the same time as crystallization of the active layer (channel forming region)." (page 2, lines 12-17); "According to the present invention,... the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18); "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)).
11. A transistor comprising:	The present invention relates to a method of obtaining... (thin film transistor or TFT) (page 1, lines 5-8); The TFT . . .was fabricated through the process described above. (page 7, line 32 – page 8, line 1)
a channel region;	"channel forming region (the semiconductor region under the gate) electrode" (page 8, lines 8-9) (Fig. 1)
a source region	"the source" (page 8, line 7).
having a source portion adjacent to the channel region; and	"[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18). As

	shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)). Thus, any "grain boundary" exists in the source portion and defines the first source portion and the second source portion.
a drain region having a drain portion adjacent to the channel region;	"[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)). Thus, any "grain boundary" exists in the drain portion and defines the first drain portion and the second drain portion.
wherein the channel region and at least one of the source portion and the drain portion comprise a metal advanced lateral crystallization region.	"[T]heir direction of crystallization is the same. (page 8, lines 9-10) "advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17.) "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction

	with the surface of the substrate" (page 24, lines 2-3).
12. A transistor comprising:	The present invention relates to a method of obtaining... (thin film transistor or TFT) (page 1, lines 5-8); The TFT . . .was fabricated through the process described above. (page 7, line 32 – page 8, line 1)
a metal-induced lateral crystallization region	"forming regions containing at least one of nickel,... so that they adhere on part of the impurity regions, and by annealing the whole to crystallize it starting from the region containing nickel" (page 2, lines 8-11). "advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17). "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction with the surface of the substrate" (page 24, lines 2-3).
formed on a substrate	substrate . . . 10 (page 6, line 11).
with a semiconductor material	title; "an amorphous silicon film" (page 6, line 12)
and including a channel region; and	"channel forming region (the semiconductor region under the gate) electrode" (page 8, lines 8-9) (Fig. 1)
a plurality of metal-induced crystallization regions formed on sides of the metal induced lateral crystallization region with a semiconductor material,	"[H]oles were created on the silicon oxide file 13 on the impurity regions to form nickel silicide (or nickel) films 17A and 17B . . . Then annealing was carried out . . to crystallize the impurity regions 16 and other semiconductor regions." (Fig. 1; page 7 lines 16-22).
wherein at least one boundary between the metal induced lateral crystallization region and one of the metal induced crystallization regions	"[T]he present invention allows substantial elimination of the grain boundary between the source and drain and the active layer... by

is located outside the channel region.	advancing the crystallization of the source and drain at the same time as crystallization of the active layer (channel forming region)." (page 2, lines 12-17); "According to the present invention,... the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18); "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)).
13. A transistor comprising:	The present invention relates to a method of obtaining... (thin film transistor or TFT) (page 1, lines 5-8); The TFT . . .was fabricated through the process described above. (page 7, line 32 – page 8, line 1)
a channel region;	"channel forming region (the semiconductor region under the gate) electrode" (page 8, lines 8-9) (Fig. 1)
a source region	"the source" (page 8, line 7).
having a first source portion adjacent to the channel region and a second source portion adjacent to the first source portion; and	"[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)). Thus, any "grain boundary" exists in the source portion and defines the first source portion and the second source portion.
a drain region having a first drain portion adjacent to the channel region and a second drain portion adjacent to the first drain portion;	"[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "crystal growth advances from both ends of the island

	semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)). Thus, any "grain boundary" exists in the drain portion and defines the first drain portion and the second drain portion.
wherein the channel region and at least one of the first source portion and the first drain portion comprise a metal induced lateral crystallization region.	"[T]heir direction of crystallization is the same. (page 8, lines 9-10) "advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17.) "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction with the surface of the substrate" (page 24, lines 2-3).